## What is Claimed is:

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- A method for addressing dynamic random access memory, with
- providing a row address and a column address to addressing terminals of the memory, in intervals provided by a timing clock signal, characterised in
  - dividing the row address and/or the column address into parts, and
  - providing the respective parts to the address terminals at a rising, and a falling edge of the timing clock signal.
- 15 2. The method of claim 1, wherein the respective parts are provided to the address terminal at consecutive rising and falling edges of the timing clock signal.
- The method of claim 1, with dividing the row address
  into two parts.
  - 4. The method of claim 3, with providing the two parts of the row address, respectively, at a first rising edge and a first falling edge within a timing cycle of the timing clock signal.
    - 5. The method of claim 1, with dividing the column address into two parts.
- 30 6. The method of claim 5, with the two parts of the column address, respectively, after a latency time for processing the row address at a first falling edge and

a following rising edge within a timing cycle of the timing clock signal.

- 7. The method of claim 6, with providing a latency of tworising edges for processing the row address.
  - 8. The method of claim 1, with dividing the row address and/or the column address into more than two parts.
- 10 9. The method of claim 8, with providing the parts of the row address at rising and falling edges at the beginning of a timing cycle of the timing clock signal, respectively.
- 15 10. The method of claim 8, with providing the parts of the column address after a latency time for processing the row address at the falling and rising edges at the end of a timing cycle of the timing clock signal, respectively.

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- 11. The method of claim 1, with providing a latency of two rising edges for processing the column address.
- 12. The method of claim 1, with processing the parts of the row address and/or the parts of the column address provided sequentially at the address terminals within the memory.
- 13. The method of claim 1, with processing parts of the row address within the memory before receiving the complete row address.
  - 14. A dynamic random access memory device comprising

 address terminals for receiving address information, and address processing means for processing received row address and column address received via the address terminal.

## 5 characterised in that

- the address processing means receive at least parts of the row address and/or column address at rising and falling edges of a timing clock signal, respectively.
- 10 15. The memory device of claim 14, where a number of address terminals T is the address bus size ADR divided by N, such that  $T = \left\lceil \frac{ADR}{N} \right\rceil$ .
- 16. The memory device of claim 15, where N is the number of parts for the row address and/or the column address .
  - 17. The memory device of claim 14, providing row data to a row buffer after the row address has been received.
- 20 18. A computer system comprising a central processing unit and a memory device, in particular according to claim 14, with
  - an address bus providing row address and column address from the central processing unit to the memory device sequentially,
  - a clocking device providing a timing clock signal with rising and falling edges,

## characterised by

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 address processing means dividing the row address and/or the column address in parts, and

- providing the respective parts to address terminals of the memory device at rising and falling edges of the timing clock signal.
- 5 19. A computer program product with a computer program stored thereon for providing address information to a memory device for accessing data within the memory device, the program comprising instructions operable to cause a processor to,
- provide a row address and a column address to addressing terminals of the memory device sequentially,

## characterised by

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- dividing the row address and/or the column address into parts, and
- providing the respective parts to the address terminals at a rising and a falling edge of a clock signal.
- 20 20. A use of a memory device of claim 14 in consumer electronic devices or mobile communication devices.
  - 21. A mobile communication device comprising a memory device of claim 14.